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EXAMINER	
TRAN, VINCENT HUY	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/037,861	YAN CHONG	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-15,17-,25 and 27-33* is/are rejected.

7)☒ Claim(s) *16 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/12/02-8/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 14-33 are pending for examination.

Claim Objections

2. Claim 22 is objected to because of the following informalities: first variable-delay circuit block should be second variable-delay circuit block. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 25 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: First – Second - Third flip-flop.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 14, 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto U.S. Patent 6,351,166 in view of Coddington et al U.S. Patent 6,140,854.

7. As per claim 14, Hashimoto teaches a integrated circuit comprising:

a series of circuits [fig. 8];

a phase detector [16 fig. 8] having a first input coupled to an input of the series of circuits [15, 18 fig. 8], and a second input couple to an output of the series of circuits;

a delay control circuit [17 fig. 8] having an input coupled to an output of the phase detector;

and first variable-delay block [12 fig. 8] having a control input couple to an output of the a delay control circuit,

wherein the series of circuits comprising:

a frequency divider [15 fig. 8];

a second variable-delay block having a control input coupled to the output of the delay control circuit.

Hashimoto teaches the phase detector circuit 16 controls the delay amount of the variable-delay circuit 12 and 18 via the delay-control circuit 17 [col. 8 lines 34-46]. However, Hashimoto does not explicitly teach the delay-control circuit as an up/down counter.

Coddington et al teach another system has a shifting delay circuit which provides a variable delay for delaying a source clock. Specifically, Coddington et al teach a delay control circuit ,as an up/down counter, generating a delay control signal based on the count, increment or decrement its count basing the phase lead/lag signal from the phase detector[col. 28-38]. At the time of the invention was made, it would have been obvious to one of ordinary skill to have modified the Hashimoto's delay control circuit with the up/down counter of Coddington et al since the up/down counter are well know in the art for delay control.

8. As per claim 17, Coddington et al teach an input of the second variable-delay block is coupled to an output of the frequency divider [162, 72 fig. 3].

9. As per claim 18, Hashimoto teaches an output of the frequency divider is coupled to an input of the second variable-delay block [15, 18 fig. 8].

10. As per claim 19, Hashimoto teaches an integrated circuit comprising:

a series combination of a first frequency divider [15 fig. 8] and a first variable-delay block circuitry [18 fig. 8], configured to receive a first clock signal [N3-14];

a phase detector configure to receive the first clock signal [16 fig. 8] and an output from the series combination [fig. 8];

an up/down counter[1] configured to receive an output from the phase detector [17-17 fig. 8]; and

a second variable-delay block [12 fig. 8]configured to receive a second clock signal [I-clk fig. 8],

wherein the first variable-delay block and the second variable-delay block are configured to receive an output form the up/down counter [output of 17 fig. 8].

[1] See discussion in claim 1.

11. As per claim 20, Hashimoto teaches the first frequency divider is configured to receive the first clock signal and the first variable-delay block is configure to receive an output from the first frequency divider [15, 18 fig. 8].

12. Claims 15, 22-24, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto and Coddington et al as applied to claim 14, 19 above, and further in view of Abdel-Hafeez et al U.S. Patent 6,356,509.

13. As per claim 15, 22, Hashimoto teaches an output circuit, which has its output couple to the memory, is coupled to the output of the first variable delay block. Hashimoto does not expressly teach the outlay of the output circuit coupled to the first delay block.

Abdel-Hafeez et al teach a system for efficiently implementing a double data rate memory architecture. Specifically, Abdel-Hafeez et al teach a first flip-flop [820 fig. 8]having a clock input couple to the memory clock [Mclock 216 (a) fig. 8. Obviously, the same clock as of output from the first variable delay block[2]]; and

the second flip-flop [836 fig. 8]having a complementary clock input coupled to the memory block [claim 15, 16].

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have combine the teachings of both Hashimoto, and Abdel-Hafeez et al since they both directed to the teaching of the synchronization signal thereby to efficiently implement data transfer processes. Abdel-Hafeez et al teach a first and second flip-flop, which configure to

[2] The circuit 14 of fig. 8[Hashimoto] generates an internal clock signal [memory clock] I-clk based on the external clock signal [system clock] which input to the first variable delay.

receive a memory clock, in order to provides a method for efficiently and effectively implementing a double data rate memory architecture [col. 2 lines 17-27].

14. As per claim 23, Abdel-Hafeez et al teach a memory configured to receive an output of the first flip-flop and an output of the second flip-flop [claim 15];

15. As per claim 24, an synchronous dynamic random access memory configured to receive an output of the first flip-flop and an output of the second flip-flop [obvious from abtract].

16. As per claim 27, Abdel-Hafeez et al teach the integrated circuit is a programmable logic device [col. 2 lines 18-28].

17. Claims 21, 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto and Coddington et al as applied to claim 14 above, and further in view of Funaba et al U.S. Patent 6212,127.

18. As per claim 21, Hashimoto teaches the first variable-delay block is configured to receive the first clock signal. However, Hashimoto does not teach the first frequency divider is configured to receive an output from the first variable-delay block.

Funaba et al teach another system relates to a timing control circuit for changing a delay of a signal employed in an electronic circuit. Specifically, Funaba et al teach the first variable-delay block [103 fig. 1] is configured to receive the first clock signal [101 fig. 1] and the first frequency divider [108 fig. 1] is configured to receive an output from the first variable-delay block.

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the Hashimoto/Coddington et al circuitry with the first frequency divider is configured to receive an output from the first variable-delay block as taught by Funaba et al in order to decrease the number of variable delay circuit, and shortening a lock-in cycle in a semiconductor device having a timing control circuit.

19. As per claim 28, Funaba et al teach a multiple-data-rate memory ; and the integrated circuit of claim 14 coupled to the multiple-data-rate memory [col. 2 lines 16-60];

20. As per claim 29, Funaba et al teach the multiple data rate memory is a double-data-rate memory [col. 2 lines 18-19].

21. Claims 30-32 rejected under 35 U.S.C. 103(a) as being unpatentable over Coddington et al in view of Takahashi U.S. Patent 6,346,843.

22. As per claim 30, Coddington et al teach an integrated circuit comprising:

a series of circuits [fig. 3] comprising:

a dividing means [162 fig. 3] for dividing a frequency of a clock signal; and

a delaying means [72 fig. 3] for delaying a clock signal by a first duration [col. 7 lines 16-19], wherein the series of circuits receives a first clock signal and provides a second clock signal [106 fig. 3], the second clock signal delayed and divided in frequency from the first clock signal;

phase detector means [76 fig. 3] for receiving the first [54 fig. 3] and second clock signals [106 fig. 3], and providing an output;

Coddington et al specifically teach an adjustment means [76-74 fig. 3] for increasing or decreasing the durations of the variable-delay line [72 fig. 3] based on the output of the phase detector means [col. 4 lines 27-40]. However, Coddington et al do not expressly teach the second delaying means for delaying a third clock signal by a second duration.

Takahashi teaches another clock signal generating circuit capable of establishing accurate synchronization between an input clock signal and an internal clock signal to prevent an input circuit from causing a synchronization shift. Specifically, Takashi teaches a second delaying means [45 fig. 4] for delaying a third clock signal [clock signal between 44 and 45] by a second duration [col. 3 lines 1-7, 19-24; col. 8 lines 14-22]. Takashi further teaches an adjustment means [42, 48 fig. 4] for increase or decreasing the first and second durations based on the output of the phase detector means [col. 14 lines 31-61].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the Coddington et al circuitry with the second delaying means for delaying a clock signal by a second duration as taught by Takahashi's circuit in order to establish an accurate synchronization between the external and internal clock signals [col. 15 lines 13-15].

23. As per claim 31, Coddington et al teach the series of circuits provides the second clock signal by first dividing the frequency of the first clock signal [162 fig. 3].

24. As per claim 32, Coddington et al teach the frequency of the first clock signal is divided by a value selected from the group consisting of 4, 8, and 16 [col. 5 lines 54-57, col. 6 lines 1-15, col. 7 lines 5-6].

25. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coddington et al and Takahashi as applied to claim 30 above, and further in view of Funaba et al U.S. Patent 6,269,051.

26. As per claim 33, Coddington et al teach the series of circuits provides the second clock signal by delaying the first clock signal after dividing its frequency. However, Coddington et al do not expressly teach the series of circuits provides the second clock signal by delaying the first clock signal before dividing its frequency.

Funaba et al teach another system relates to a timing control circuit for changing a delay of a signal employed in an electronic circuit. Specifically, Funaba et al teach the series of circuits provides the second clock signal by delaying the first clock signal before dividing its frequency [103, 108, 111 fig. 1]. At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the Coddington et al circuitry with the delaying of the first clock signal before dividing its frequency as taught by Funaba et al in order to decrease the number of variable delay circuit, and shortening a lock-in cycle in a semiconductor device having a timing control circuit.

Allowable Subject Matter

27. Claims 16, 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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